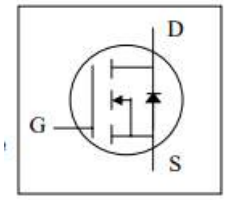
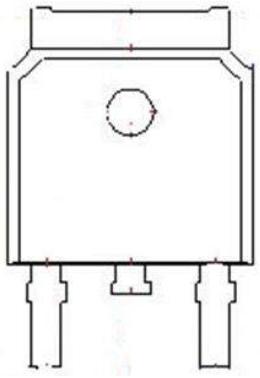
9N50D

500V N-Channel Enhancement Mode MOSFET

Description

The 9N50D is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.





General Features

VDS =500V,ID =9A

RDS(ON) <0.84Ω@ VGS=10V

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)

Absolute Maximum Ratings (T_C=25℃ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		500	V
V_{GSS}	Gate-Source Voltage		±30	V
I_D	Continuous Drain Current	T_C = 25℃	9	A
		T_C = 100℃	5.4	A
I_{DM}	Pulsed Drain Current note1		36	A
E_{AS}	Single Pulsed Avalanche Energy note2		198	mJ
P_D	Power Dissipation	T_C = 25℃	150	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.25	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		100	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics (T_C=25℃ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS} = 0V,I_D = 250μA	500	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V, T_J = 25℃	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	V_{GS} =0V, V_{GS} = ±30V	-	-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} =V_{GS},I_D = 250μA	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note3	V_{GS} =10V, I_D =4.5A	-	0.67	0.84	Ω
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	-	891	-	pF
C_{oss}	Output Capacitance		-	110	-	pF
C_{rss}	Reverse Transfer Capacitance		-	14	-	pF
Q_g	Total Gate Charge	V_{DD}=400V, I_D =9A, V_{GS} =10V	-	22	-	nC
Q_{gs}	Gate-Source Charge		-	4.3	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	13	-	nC
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250V, I_D =9A, R_G =25Ω	-	15	-	ns
t_r	Turn-On Rise Time		-	18	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	80	-	ns
t_f	Turn-Off Fall Time		-	35	-	ns
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	9	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	36	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD}=9A, T_J = 25℃	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S =9A, di/dt =100A/μs	-	300	-	ns
Q_{rr}	Reverse Recovery Charge		-	4.1	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 4.5A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Performance Characteristics

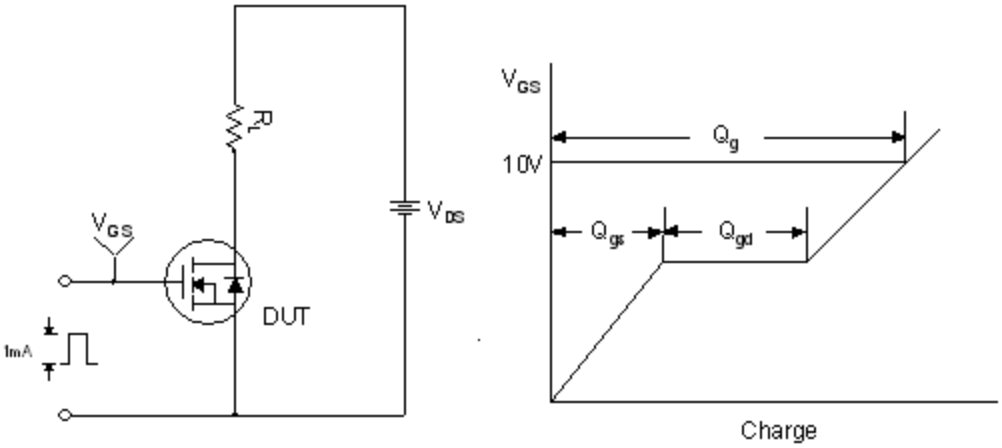


Figure 1. Gate Charge Test Circuit & Waveform

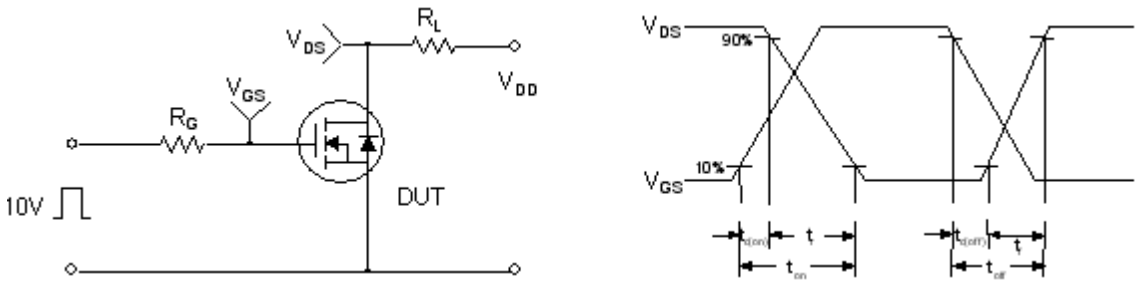


Figure 2. Resistive Switching Test Circuit & Waveforms

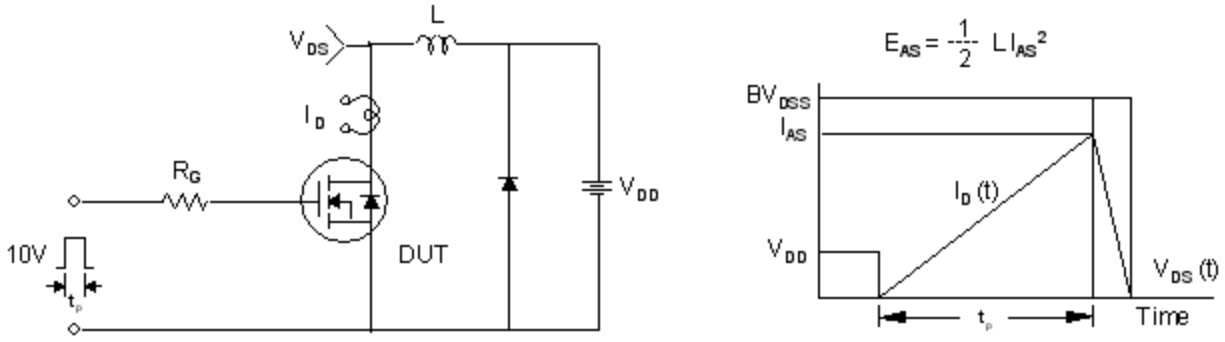
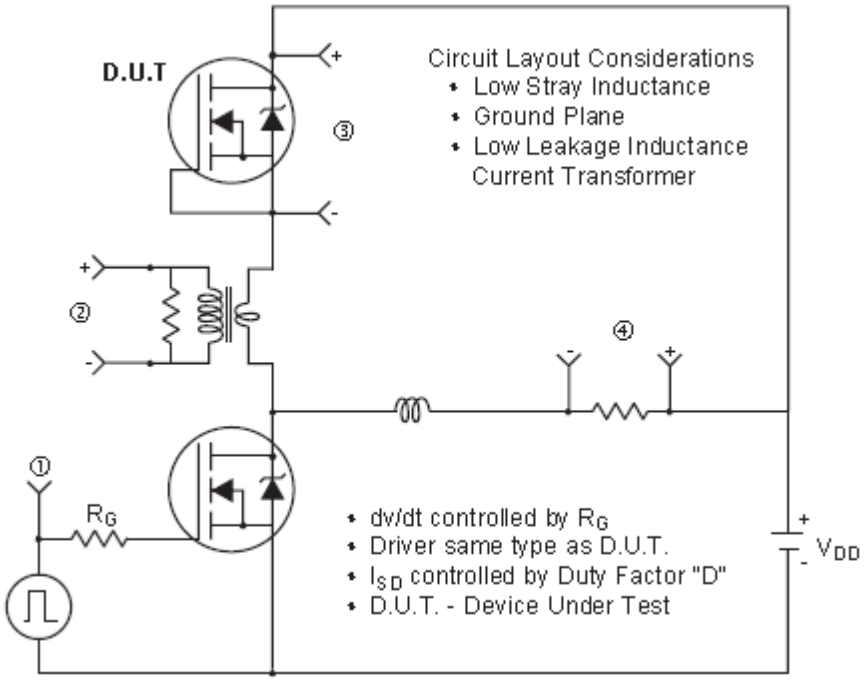


Figure 3. Unclamped Inductive Switching Test Circuit & Waveforms



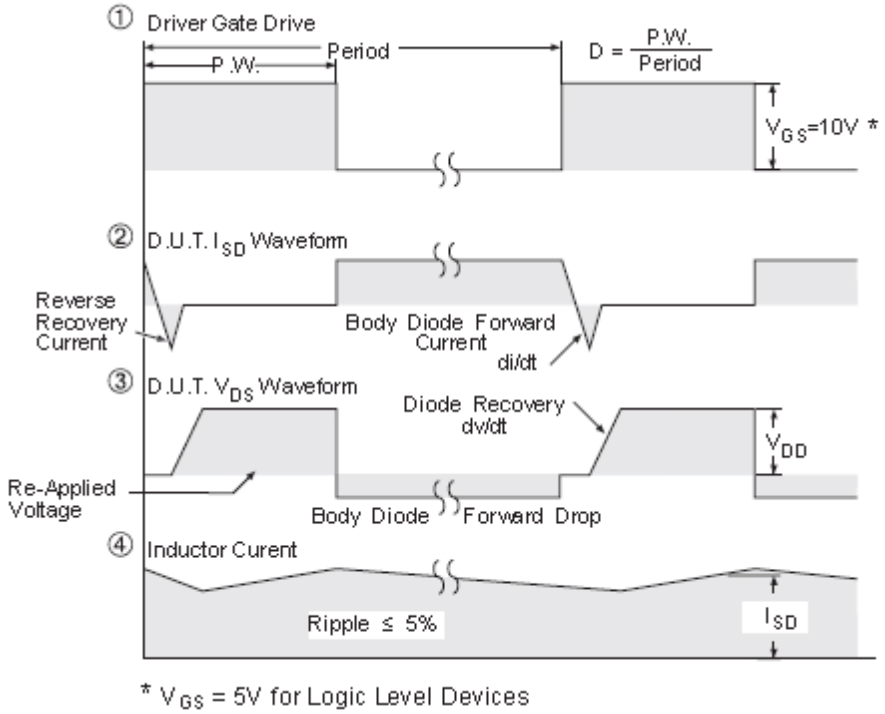
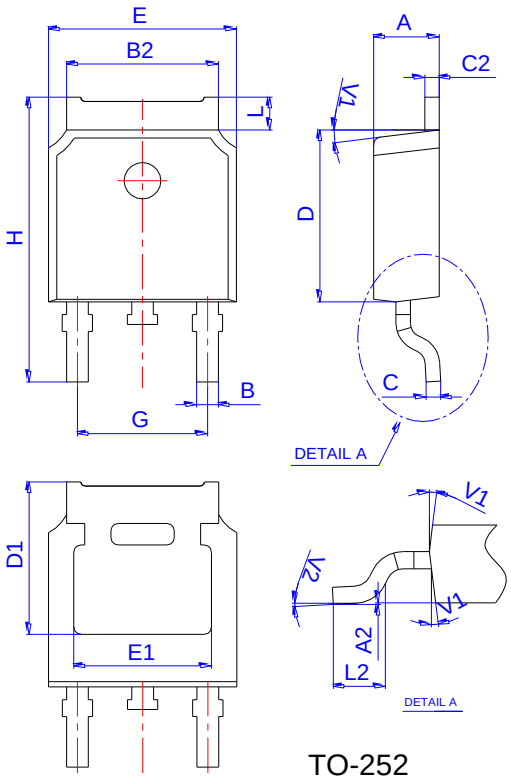


Figure 4. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

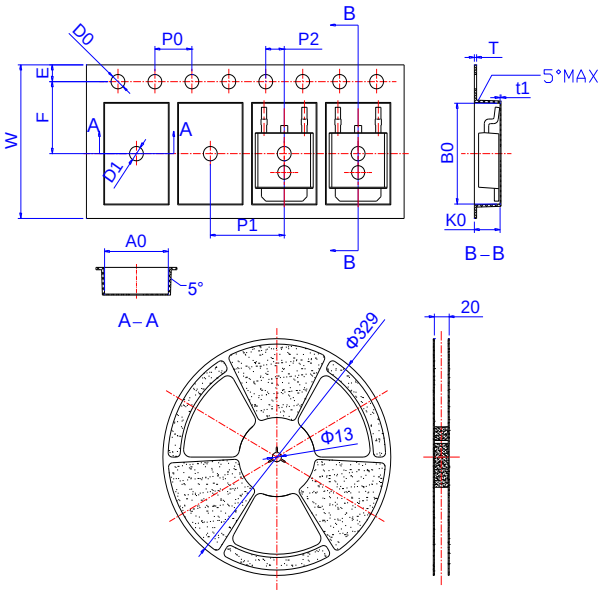
Package Mechanical Data



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

OUTLINE	REEL (PCS)	PER CARTON (PCS)	TAPE & REEL
TAPING	2,500	25,000	13inch